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MS-7390

ATX Version: 0A

CPU: AMD AM2& AM2+ Socket940
AM2 89W (3000+~6000+)
AM2+ up to 95W


System Chipset:
nVIDIA MCP65P(NF570LT-SLI)

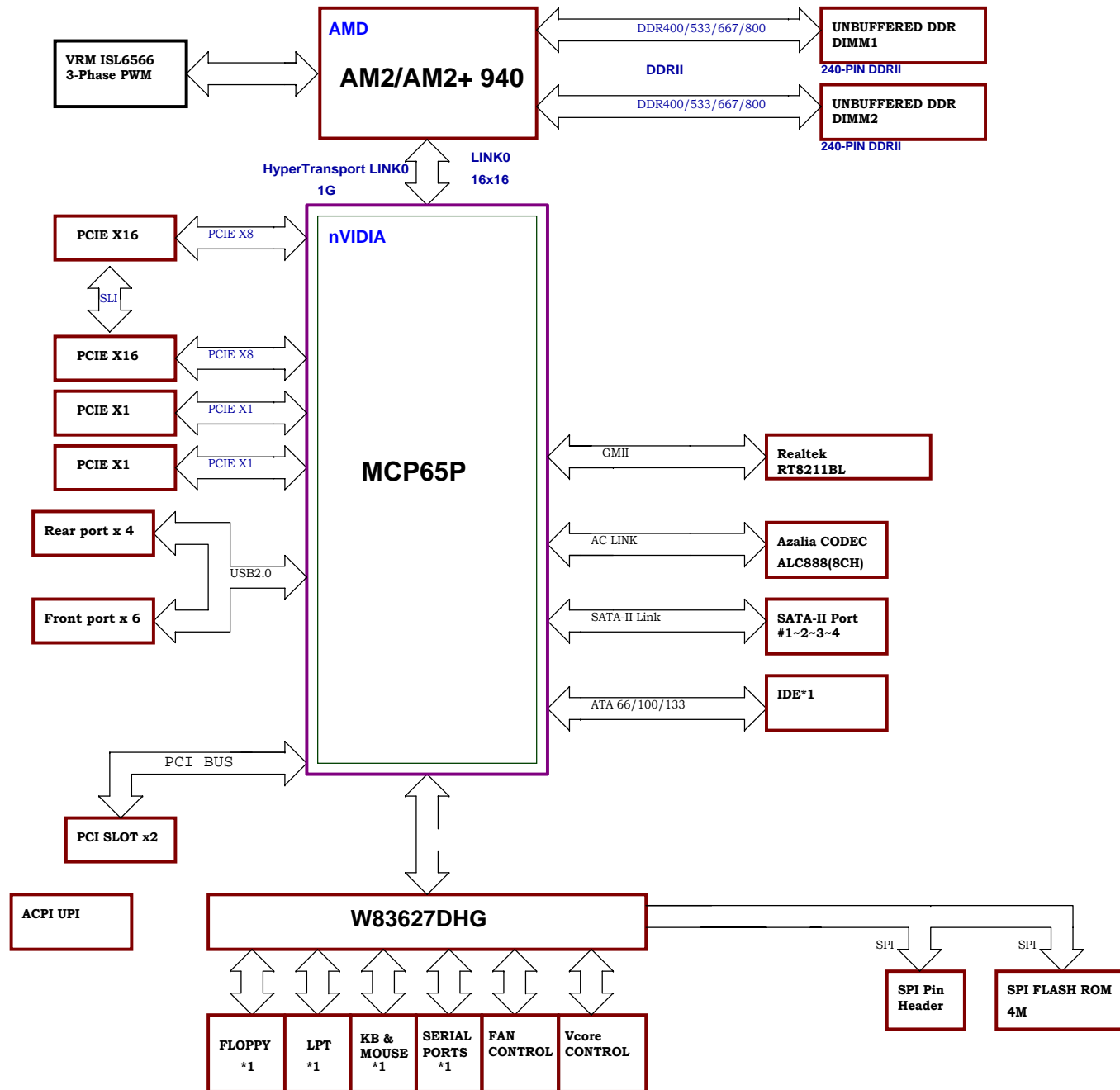
On Board Device:
LPC Super I/O -- Fintek F71882F
LAN -- Realtek 8211BL (PHY)
HD Audio Codec -- ALC888

Main Memory:
Dual-channel DDR-II *4

Expansion Slots:
PCI EXPRESS X16 SLOT *2(Real X8)-SLI
PCI EXPRESS X1 SLOT * 2
PCI SLOT * 2

PWM: Intersil ISL6566 (3Phases)

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Title			
Cover Page			
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6.7 MEM_MA_DQS_L[7..0] >> MEM_MA_DATA[63..0] 6.7
6.7 MEM_MA_DQS_H[7..0] >>
6.7 MEM_MA_DM[7..0] >>
6.7.8 MEM_MA_ADD[15..0] >>

6.7 MEM_MB_DQS_L[7..0] >> MEM_MB_DATA[63..0] 6.7
6.7 MEM_MB_DQS_H[7..0] >>
6.7 MEM_MB_DM[7..0] >>
6.7.8 MEM_MB_ADD[15..0] >>

CPU1B

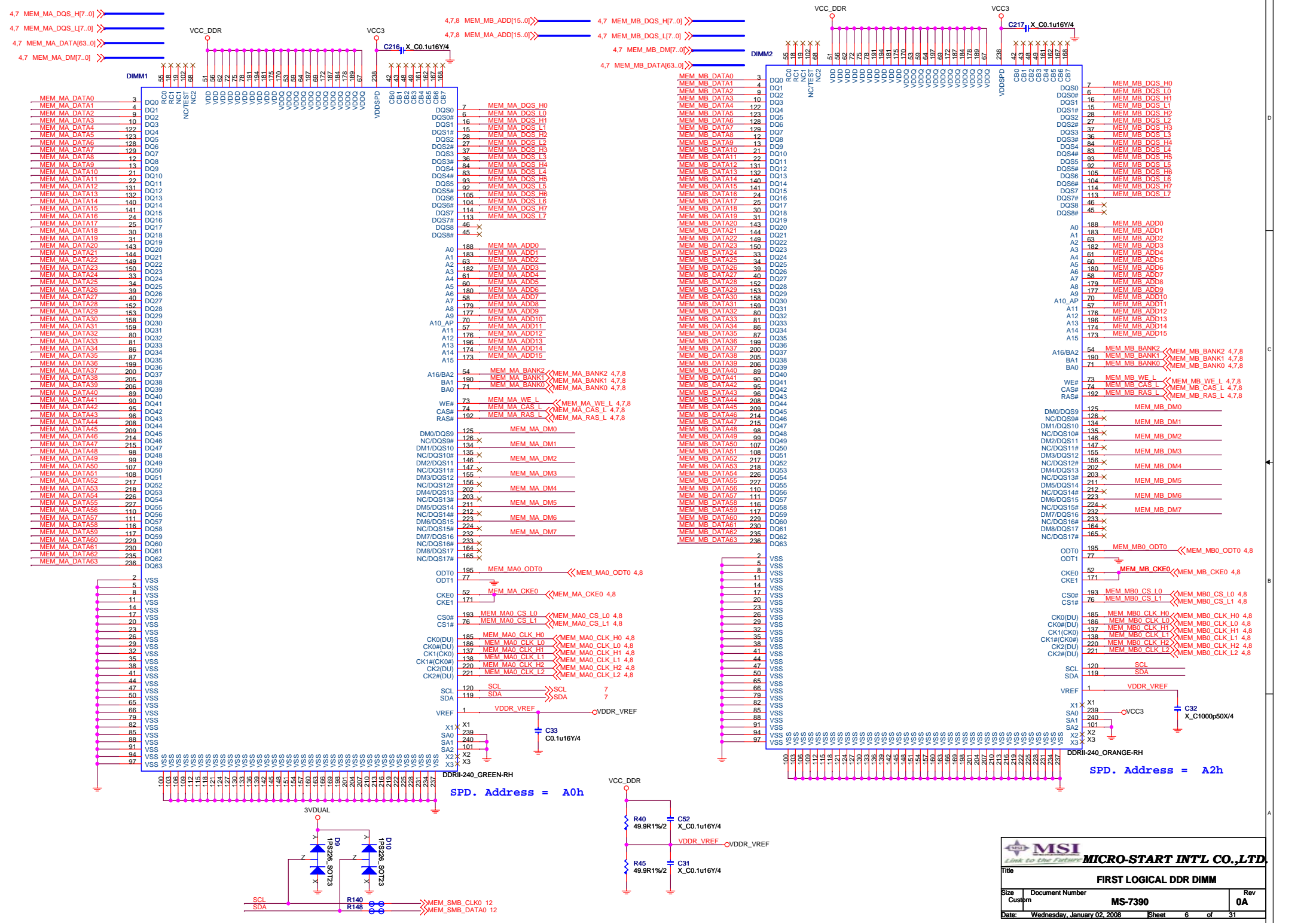
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6.8 MEM_MA0_CLK_L2	>> MEM_MA0_CLK_L2	AG20	MA0_CLK_L(2)	MA_DATA(62)	AG14	MEM_MA_DATA62
6.8 MEM_MA0_CLK_H1	>> MEM_MA0_CLK_H1	G19	MA0_CLK_H(1)	MA_DATA(61)	AG16	MEM_MA_DATA61
6.8 MEM_MA0_CLK_L1	>> MEM_MA0_CLK_L1	H19	MA0_CLK_L(1)	MA_DATA(60)	AD17	MEM_MA_DATA60
6.8 MEM_MA0_CLK_H0	>> MEM_MA0_CLK_H0	U27	MA0_CLK_H(0)	MA_DATA(59)	AD13	MEM_MA_DATA59
6.8 MEM_MA0_CLK_L0	>> MEM_MA0_CLK_L0	U26	MA0_CLK_L(0)	MA_DATA(58)	AE13	MEM_MA_DATA58
				MA_DATA(57)	AG15	MEM_MA_DATA57
6.8 MEM_MA0_CS_L1	>> MEM_MA0_CS_L1	AC25	MA0_CS_L(1)	MA_DATA(56)	AE16	MEM_MA_DATA56
6.8 MEM_MA0_CS_L0	>> MEM_MA0_CS_L0	AA24	MA0_CS_L(0)	MA_DATA(55)	AG17	MEM_MA_DATA55
				MA_DATA(54)	AE18	MEM_MA_DATA54
6.8 MEM_MA0_ODT0	>> MEM_MA0_ODT0	AC28	MA0_ODT(0)	MA_DATA(53)	AD21	MEM_MA_DATA53
				MA_DATA(52)	AG22	MEM_MA_DATA52
7.8 MEM_MA1_CLK_H2	>> MEM_MA1_CLK_H2	AE20	MA1_CLK_H(2)	MA_DATA(51)	AE17	MEM_MA_DATA51
7.8 MEM_MA1_CLK_L2	>> MEM_MA1_CLK_L2	AE19	MA1_CLK_L(2)	MA_DATA(50)	AE17	MEM_MA_DATA50
7.8 MEM_MA1_CLK_H1	>> MEM_MA1_CLK_H1	G20	MA1_CLK_H(1)	MA_DATA(49)	AE21	MEM_MA_DATA49
7.8 MEM_MA1_CLK_L1	>> MEM_MA1_CLK_L1	V27	MA1_CLK_L(1)	MA_DATA(48)	AE23	MEM_MA_DATA48
7.8 MEM_MA1_CLK_H0	>> MEM_MA1_CLK_H0	V27	MA1_CLK_H(0)	MA_DATA(47)	AE23	MEM_MA_DATA47
7.8 MEM_MA1_CLK_L0	>> MEM_MA1_CLK_L0	W27	MA1_CLK_L(0)	MA_DATA(46)	AE23	MEM_MA_DATA46
				MA_DATA(45)	AJ26	MEM_MA_DATA45
7.8 MEM_MA1_CS_L1	>> MEM_MA1_CS_L1	AD27	MA1_CS_L(1)	MA_DATA(44)	AG26	MEM_MA_DATA44
7.8 MEM_MA1_CS_L0	>> MEM_MA1_CS_L0	AA25	MA1_CS_L(0)	MA_DATA(43)	AG23	MEM_MA_DATA43
				MA_DATA(42)	AH25	MEM_MA_DATA42
7.8 MEM_MA1_ODT0	>> MEM_MA1_ODT0	AC27	MA1_ODT(0)	MA_DATA(41)	AF25	MEM_MA_DATA41
				MA_DATA(40)	AJ28	MEM_MA_DATA39
6.7.8 MEM_MA_CAS_L	>> MEM_MA_CAS_L	AB25	MA_CAS_L	MA_DATA(38)	AJ29	MEM_MA_DATA38
6.7.8 MEM_MA_WE_L	>> MEM_MA_WE_L	AB27	MA_WE_L	MA_DATA(37)	AF29	MEM_MA_DATA37
6.7.8 MEM_MA_RAS_L	>> MEM_MA_RAS_L	AA26	MA_RAS_L	MA_DATA(36)	AJ27	MEM_MA_DATA36
6.7.8 MEM_MA_BANK2	>> MEM_MA_BANK2	N25	MA_BANK(2)	MA_DATA(35)	AH27	MEM_MA_DATA35
6.7.8 MEM_MA_BANK1	>> MEM_MA_BANK1	Y27	MA_BANK(1)	MA_DATA(34)	AG29	MEM_MA_DATA34
6.7.8 MEM_MA_BANK0	>> MEM_MA_BANK0	AA27	MA_BANK(0)	MA_DATA(32)	AE27	MEM_MA_DATA32
				MA_DATA(31)	E28	MEM_MA_DATA31
7.8 MEM_MA_CKE1	>> MEM_MA_CKE1	L27	MA_CKE(1)	MA_DATA(30)	D27	MEM_MA_DATA29
6.8 MEM_MA_CKE0	>> MEM_MA_CKE0	M25	MA_CKE(0)	MA_DATA(28)	C27	MEM_MA_DATA28
				MA_DATA(27)	G26	MEM_MA_DATA27
				MA_DATA(26)	F27	MEM_MA_DATA26
				MA_DATA(25)	C28	MEM_MA_DATA25
				MA_DATA(24)	E27	MEM_MA_DATA24
				MA_DATA(23)	F25	MEM_MA_DATA23
				MA_DATA(22)	E25	MEM_MA_DATA22
				MA_DATA(21)	E23	MEM_MA_DATA21
				MA_DATA(20)	D23	MEM_MA_DATA20
				MA_DATA(19)	C26	MEM_MA_DATA19
				MA_DATA(18)	G23	MEM_MA_DATA17
				MA_DATA(17)	F23	MEM_MA_DATA16
				MA_DATA(16)	E22	MEM_MA_DATA15
				MA_DATA(15)	E21	MEM_MA_DATA14
				MA_DATA(14)	F17	MEM_MA_DATA13
				MA_DATA(13)	G17	MEM_MA_DATA12
				MA_DATA(12)	G22	MEM_MA_DATA11
				MA_DATA(11)	F21	MEM_MA_DATA10
				MA_DATA(10)	G18	MEM_MA_DATA9
				MA_DATA(9)	E17	MEM_MA_DATA8
				MA_DATA(8)	F16	MEM_MA_DATA7
				MA_DATA(7)	G16	MEM_MA_DATA6
				MA_DATA(6)	G13	MEM_MA_DATA5
				MA_DATA(5)	H13	MEM_MA_DATA4
				MA_DATA(4)	H17	MEM_MA_DATA3
				MA_DATA(3)	E16	MEM_MA_DATA2
				MA_DATA(2)	E14	MEM_MA_DATA1
				MA_DATA(1)	G14	MEM_MA_DATA0
				MA_DATA(0)		
				MA_DQS_H(8)	J28	X
				MA_DQS_L(8)	J27	X
				MA_DQS_H(0)	J25	X
				MA_DQS_L(0)		
				MA_DM(8)		
				MA_DM(7)	K25	X
				MA_DM(6)	J26	X
				MA_DM(5)	G28	X
				MA_DM(4)	G27	X
				MA_DM(3)	L24	X
				MA_DM(2)	K27	X
				MA_DM(1)	H29	X
				MA_DM(0)	H27	X

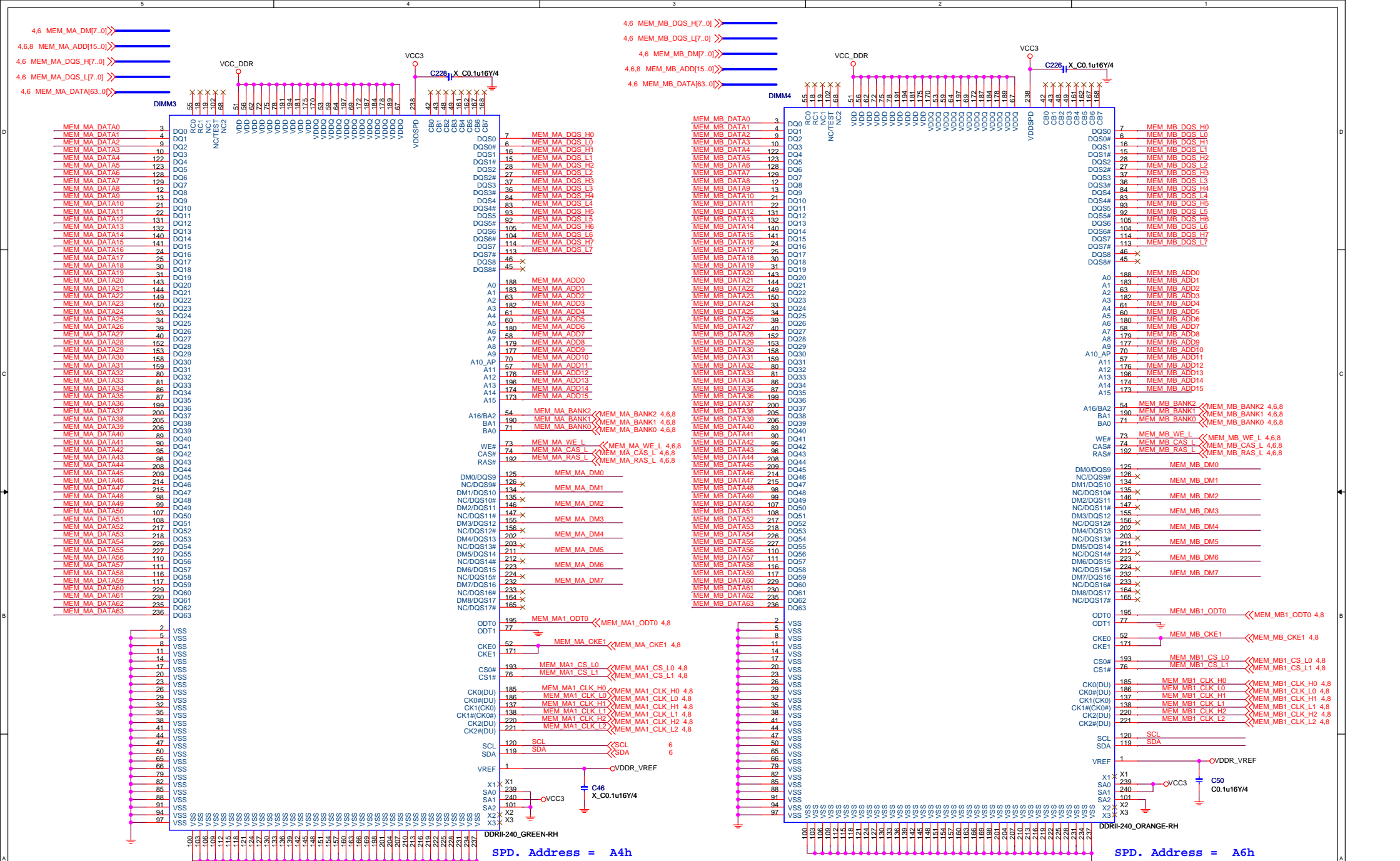
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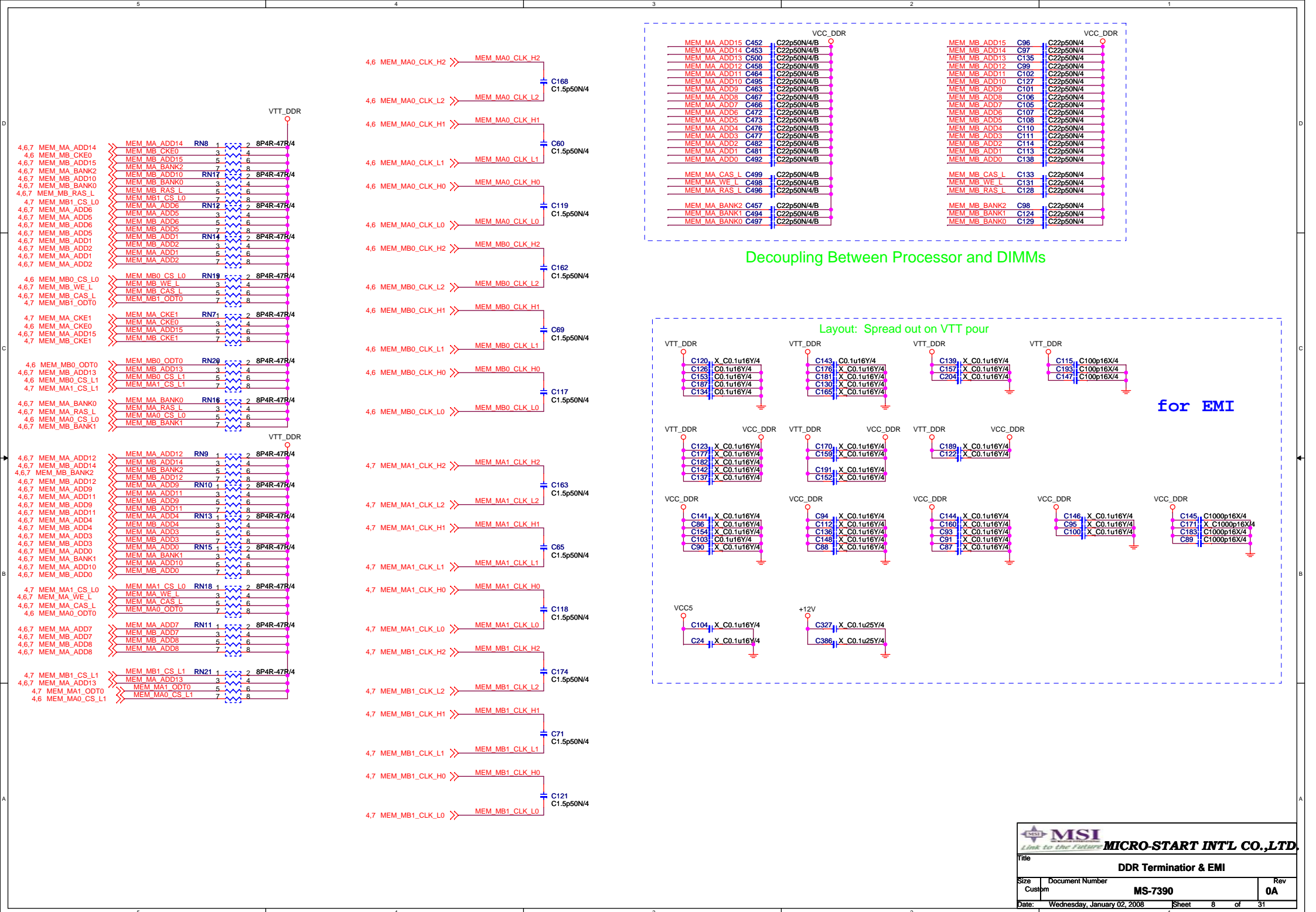
CPU1C

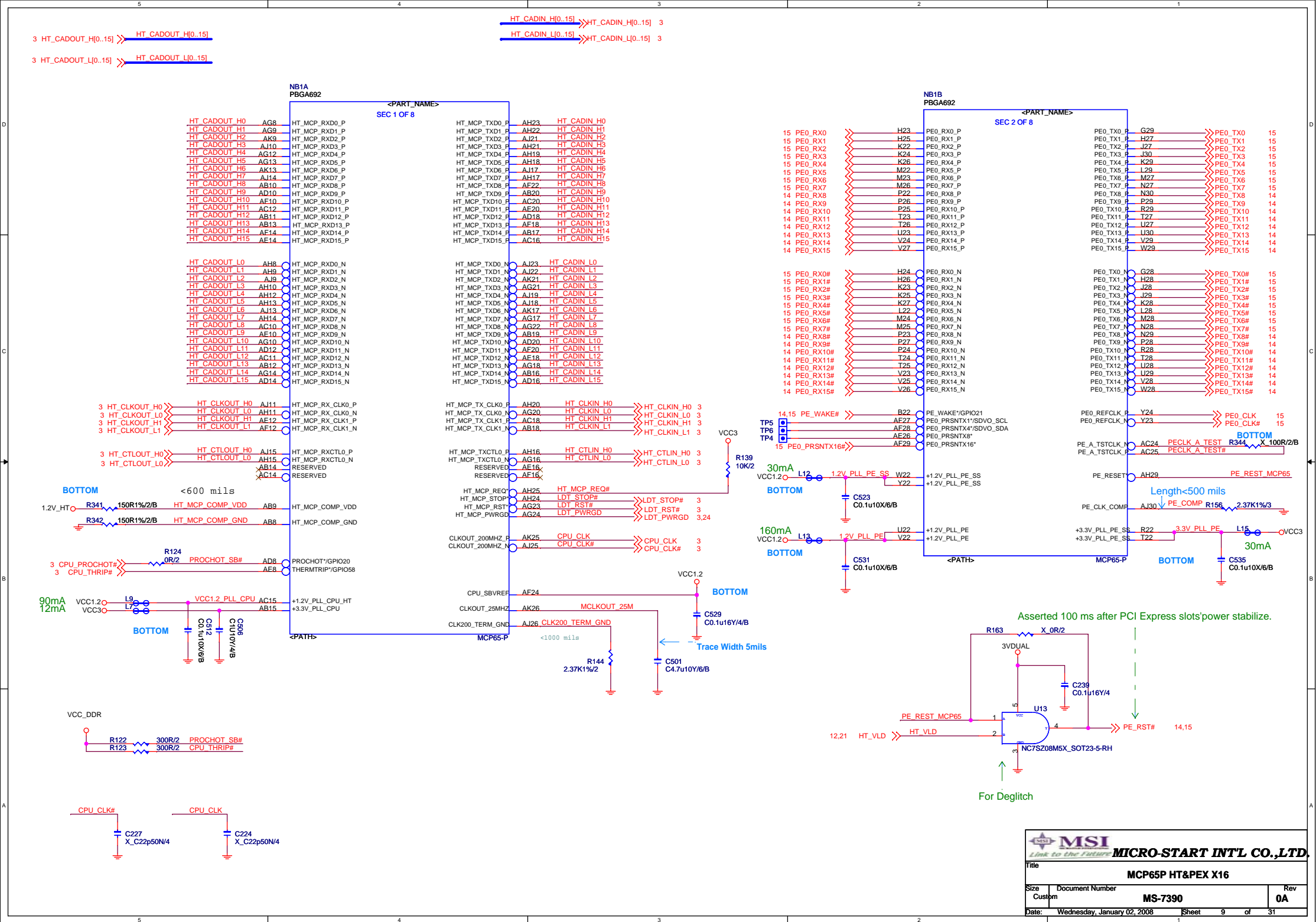
6.8 MEM_MB0_CLK_H2	>> MEM_MB0_CLK_H2	AJ19	MB0_CLK_H(2)	MB_DATA(63)	AH13	MEM_MB_DATA63
6.8 MEM_MB0_CLK_L2	>> MEM_MB0_CLK_L2	AK19	MB0_CLK_L(2)	MB_DATA(62)	AH13	MEM_MB_DATA62
6.8 MEM_MB0_CLK_H1	>> MEM_MB0_CLK_H1	A18	MB0_CLK_H(1)	MB_DATA(61)	AJ15	MEM_MB_DATA61
6.8 MEM_MB0_CLK_L1	>> MEM_MB0_CLK_L1	A19	MB0_CLK_L(1)	MB_DATA(60)	AJ15	MEM_MB_DATA60
6.8 MEM_MB0_CLK_H0	>> MEM_MB0_CLK_H0	U31	MB0_CLK_H(0)	MB_DATA(59)	AF13	MEM_MB_DATA59
6.8 MEM_MB0_CLK_L0	>> MEM_MB0_CLK_L0	U30	MB0_CLK_L(0)	MB_DATA(58)	AG13	MEM_MB_DATA58
				MB_DATA(57)	AL14	MEM_MB_DATA57
6.8 MEM_MB0_CS_L1	>> MEM_MB0_CS_L1	AE30	MB0_CS_L(1)	MB_DATA(56)	AL16	MEM_MB_DATA56
6.8 MEM_MB0_CS_L0	>> MEM_MB0_CS_L0	AC31	MB0_CS_L(0)	MB_DATA(55)	AL17	MEM_MB_DATA55
				MB_DATA(54)	AK21	MEM_MB_DATA54
6.8 MEM_MB0_ODT0	>> MEM_MB0_ODT0	AD29	MB0_ODT(0)	MB_DATA(53)	AK21	MEM_MB_DATA53
				MB_DATA(52)	AL21	MEM_MB_DATA52
7.8 MEM_MB1_CLK_H2	>> MEM_MB1_CLK_H2	AL19	MB1_CLK_H(2)	MB_DATA(51)	AH15	MEM_MB_DATA51
7.8 MEM_MB1_CLK_L2	>> MEM_MB1_CLK_L2	AL18	MB1_CLK_L(2)	MB_DATA(50)	AH19	MEM_MB_DATA50
7.8 MEM_MB1_CLK_H1	>> MEM_MB1_CLK_H1	C19	MB1_CLK_H(1)	MB_DATA(49)	AJ10	MEM_MB_DATA49
7.8 MEM_MB1_CLK_L1	>> MEM_MB1_CLK_L1	D19	MB1_CLK_L(1)	MB_DATA(48)	AL20	MEM_MB_DATA48
7.8 MEM_MB1_CLK_H0	>> MEM_MB1_CLK_H0	W29	MB1_CLK_H(0)	MB_DATA(47)	AJ22	MEM_MB_DATA47
7.8 MEM_MB1_CLK_L0	>> MEM_MB1_CLK_L0	W28	MB1_CLK_L(0)	MB_DATA(46)	AJ22	MEM_MB_DATA46
				MB_DATA(45)	AL24	MEM_MB_DATA45
7.8 MEM_MB1_CS_L1	>> MEM_MB1_CS_L1	AE29	MB1_CS_L(1)	MB_DATA(44)	AK25	MEM_MB_DATA44
7.8 MEM_MB1_CS_L0	>> MEM_MB1_CS_L0	AB31	MB1_CS_L(0)	MB_DATA(43)	AH21	MEM_MB_DATA43
				MB_DATA(42)	AH23	MEM_MB_DATA42
7.8 MEM_MB1_ODT0	>> MEM_MB1_ODT0	AD31	MB1_ODT(0)	MB_DATA(41)	AJ24	MEM_MB_DATA41
				MB_DATA(40)	AJ24	MEM_MB_DATA40
6.7.8 MEM_MB_CAS_L	>> MEM_MB_CAS_L	AC29	MB_CAS_L	MB_DATA(39)	AK27	MEM_MB_DATA39
6.7.8 MEM_MB_WE_L	>> MEM_MB_WE_L	AB29	MB_WE_L	MB_DATA(38)	AH31	MEM_MB_DATA38
6.7.8 MEM_MB_RAS_L	>> MEM_MB_RAS_L		MB_RAS_L	MB_DATA(37)	AG30	MEM_MB_DATA37
				MB_DATA(36)	AL25	MEM_MB_DATA36
6.7.8 MEM_MB_BANK2	>> MEM_MB_BANK2	N31	MB_BANK(2)	MB_DATA(35)	AL26	MEM_MB_DATA35
6.7.8 MEM_MB_BANK1	>> MEM_MB_BANK1	AA31	MB_BANK(1)	MB_DATA(34)	AJ30	MEM_MB_DATA34
6.7.8 MEM_MB_BANK0	>> MEM_MB_BANK0	AA28	MB_BANK(0)	MB_DATA(33)	AJ31	MEM_MB_DATA33
				MB_DATA(32)	E31	MEM_MB_DATA32
7.8 MEM_MB_CKE1	>> MEM_MB_CKE1	M31	MB_CKE(1)	MB_DATA(31)	E30	MEM_MB_DATA31
6.8 MEM_MB_CKE0	>> MEM_MB_CKE0	M29	MB_CKE(0)	MB_DATA(30)	B27	MEM_MB_DATA29
				MB_DATA(29)	A27	MEM_MB_DATA28
				MB_DATA(28)	F29	MEM_MB_DATA27
				MB_DATA(27)	F31	MEM_MB_DATA26
				MB_DATA(26)	A29	MEM_MB_DATA25
				MB_DATA(25)	A28	MEM_MB_DATA24
				MB_DATA(24)	A25	MEM_MB_DATA23
				MB_DATA(23)	A24	MEM_MB_DATA22
				MB_DATA(22)	C22	MEM_MB_DATA21
				MB_DATA(21)	D21	MEM_MB_DATA20
				MB_DATA(20)	B26	MEM_MB_DATA19
				MB_DATA(19)	B25	MEM_MB_DATA18
				MB_DATA(18)	B23	MEM_MB_DATA17
				MB_DATA(17)	A22	MEM_MB_DATA16
				MB_DATA(16)	B21	MEM_MB_DATA15
				MB_DATA(15)	C16	MEM_MB_DATA14
				MB_DATA(14)	D15	MEM_MB_DATA13
				MB_DATA(13)	D15	MEM_MB_DATA12
				MB_DATA(12)	C21	MEM_MB_DATA11
				MB_DATA(11)	A21	MEM_MB_DATA10
				MB_DATA(10)	A17	MEM_MB_DATA9
				MB_DATA(9)	A16	MEM_MB_DATA8
				MB_DATA(8)	B15	MEM_MB_DATA7
				MB_DATA(7)	A14	MEM_MB_DATA6
				MB_DATA(6)	E13	MEM_MB_DATA5
				MB_DATA(5)	F13	MEM_MB_DATA4
				MB_DATA(4)	C15	MEM_MB_DATA3
				MB_DATA(3)	A15	MEM_MB_DATA2
				MB_DATA(2)	D13	MEM_MB_DATA1
				MB_DATA(1)	D13	MEM_MB_DATA0
				MB_DATA(0)		
				MB_DQS_H(7)	J31	X
				MB_DQS_L(7)	J30	X
				MB_DQS_H(6)		
				MB_DQS_L(6)	J29	X
				MB_DQS_H(5)		
				MB_DQS_L(5)		
				MB_DQS_H(4)		
				MB_DQS_L(4)		
				MB_DQS_H(3)		
				MB_DQS_L(3)		
				MB_DQS_H(2)		
				MB_DQS_L(2)		
				MB_DQS_H(1)		
				MB_DQS_L(1)		
				MB_DQS_H(0)		
				MB_DQS_L(0)		
				MB_DM(8)		
				MB_DM(7)	K29	X
				MB_DM(6)	K31	X
				MB_DM(5)	G30	X
				MB_DM(4)	G29	X
				MB_DM(3)	L28	X
				MB_DM(2)	L28	X
				MB_DM(1)	H31	X
				MB_DM(0)	G31	X

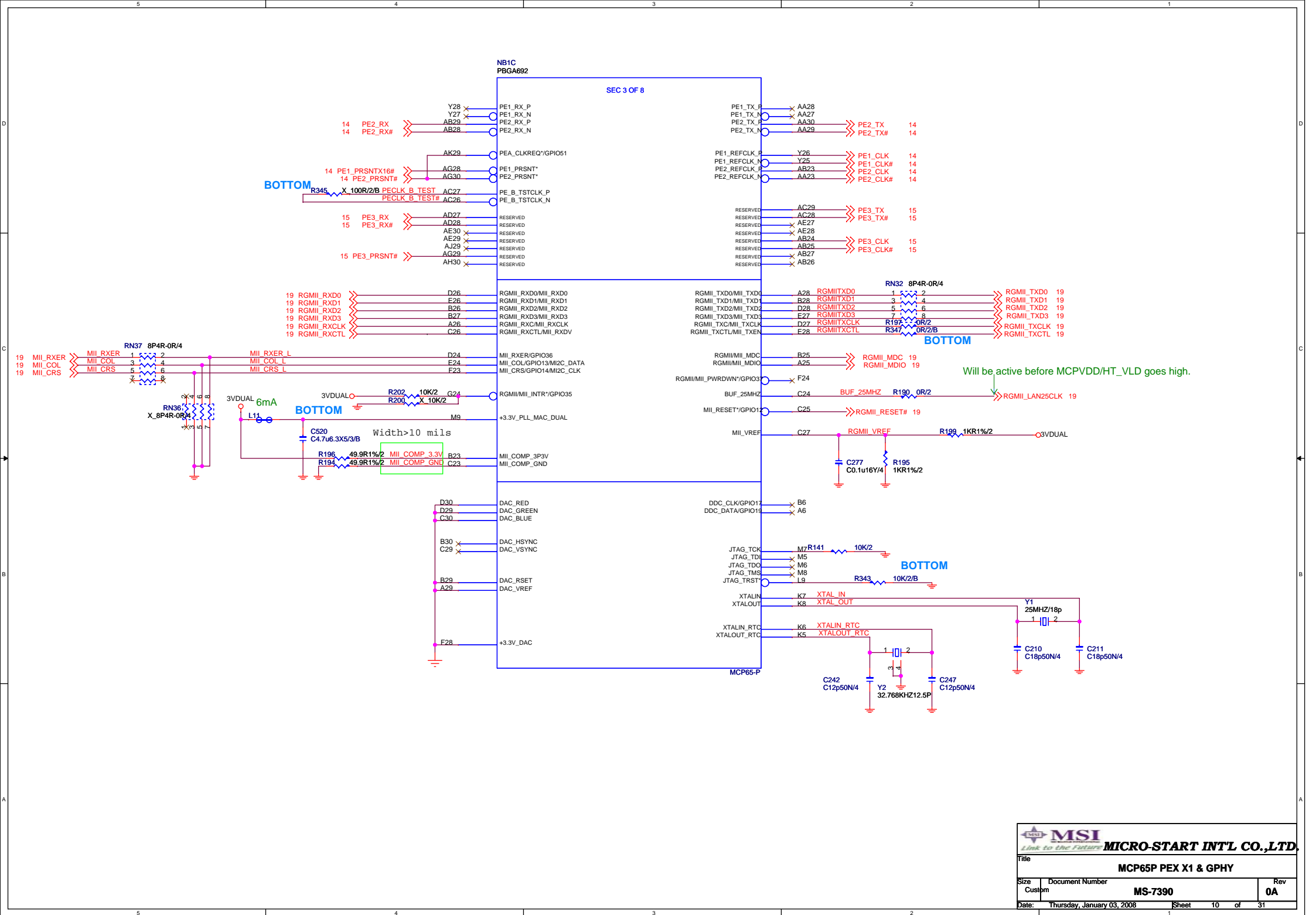
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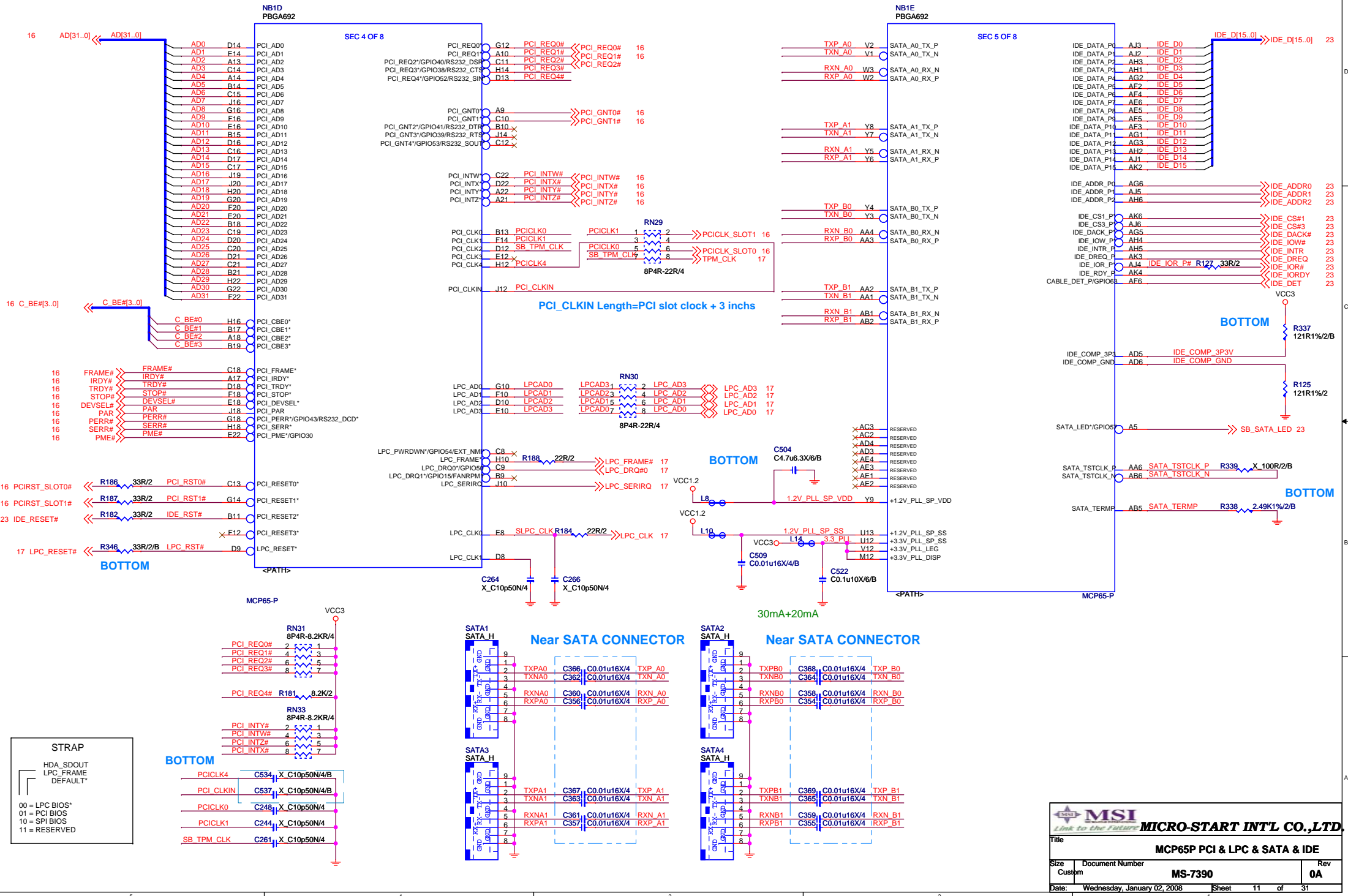






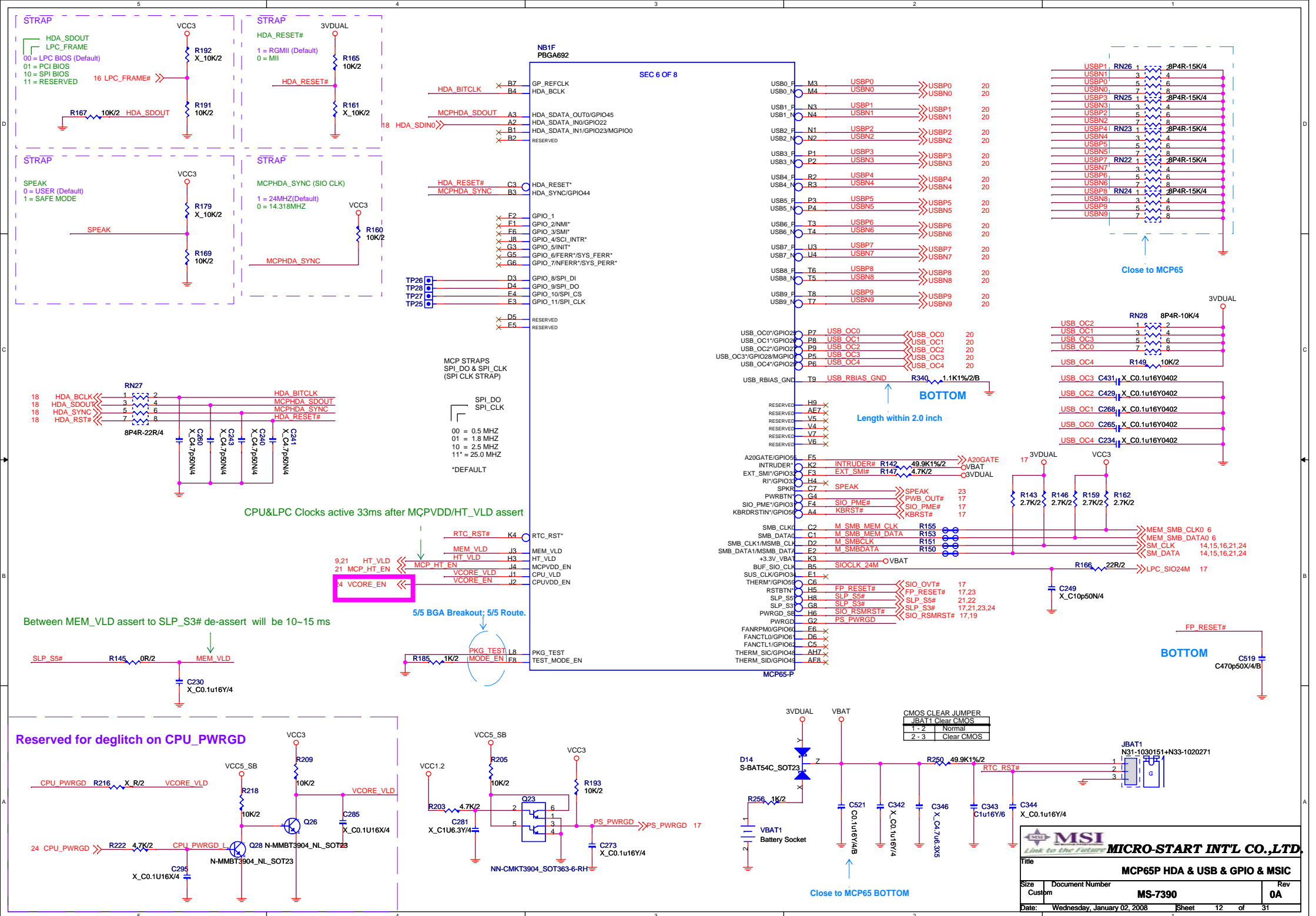


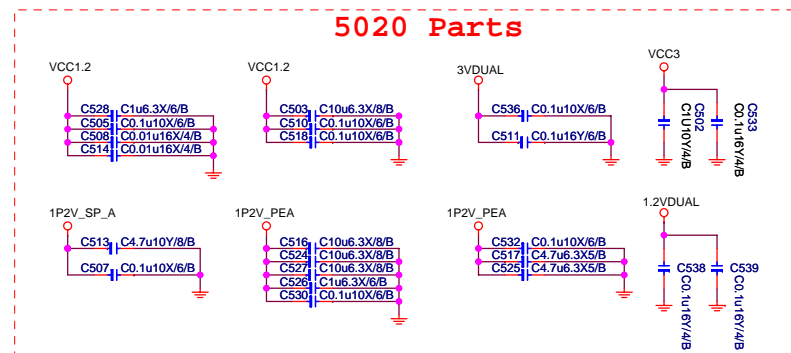
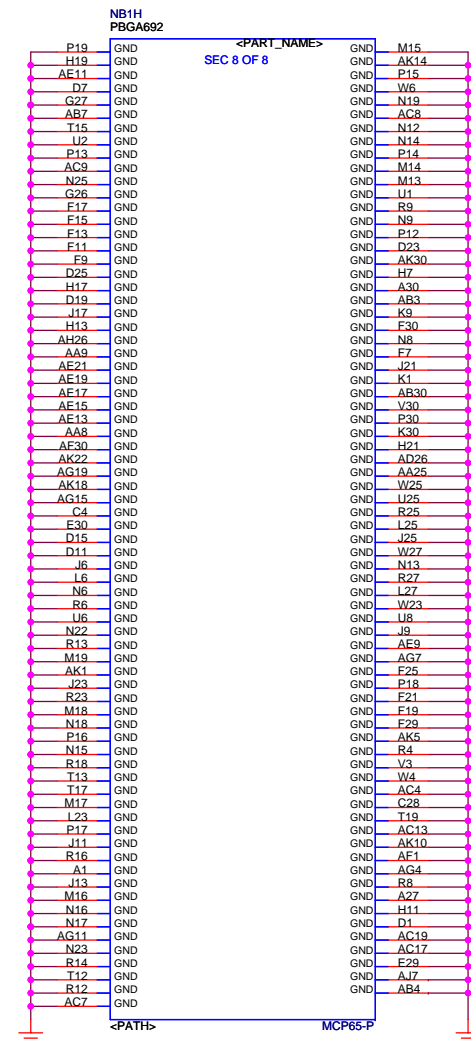




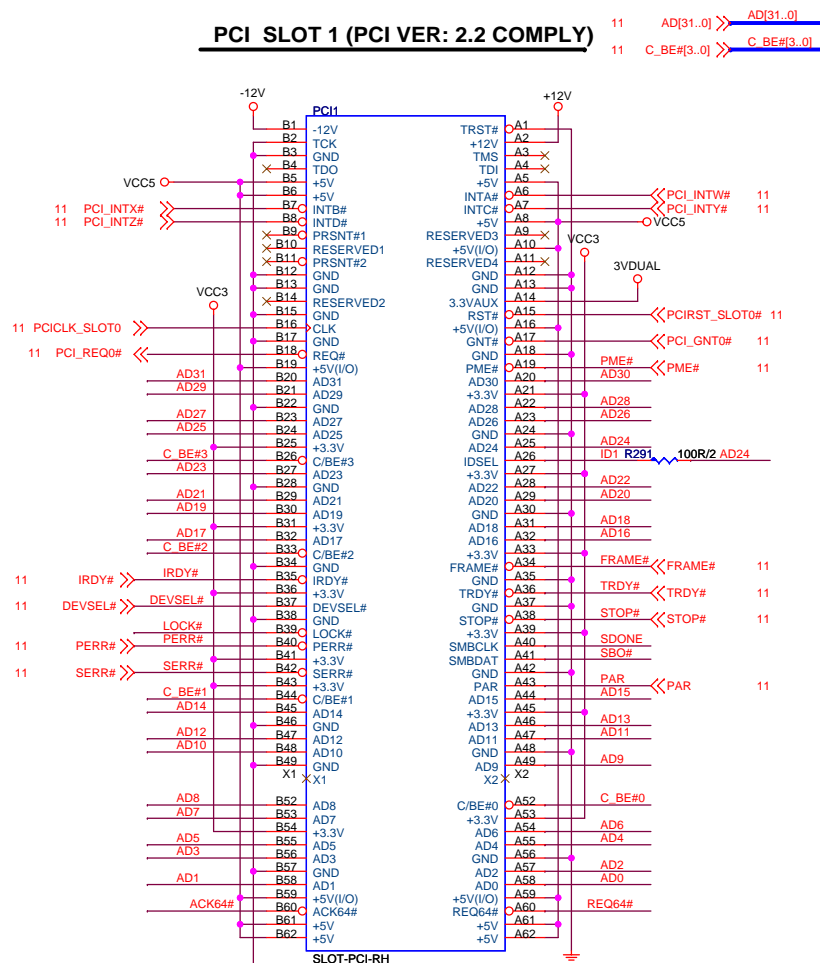
STRAP
HDA_SDOUT
LPC_FRAME
DEFAULT*

00 = LPC BIOS*
01 = PCI BIOS
10 = SPI BIOS
11 = RESERVED



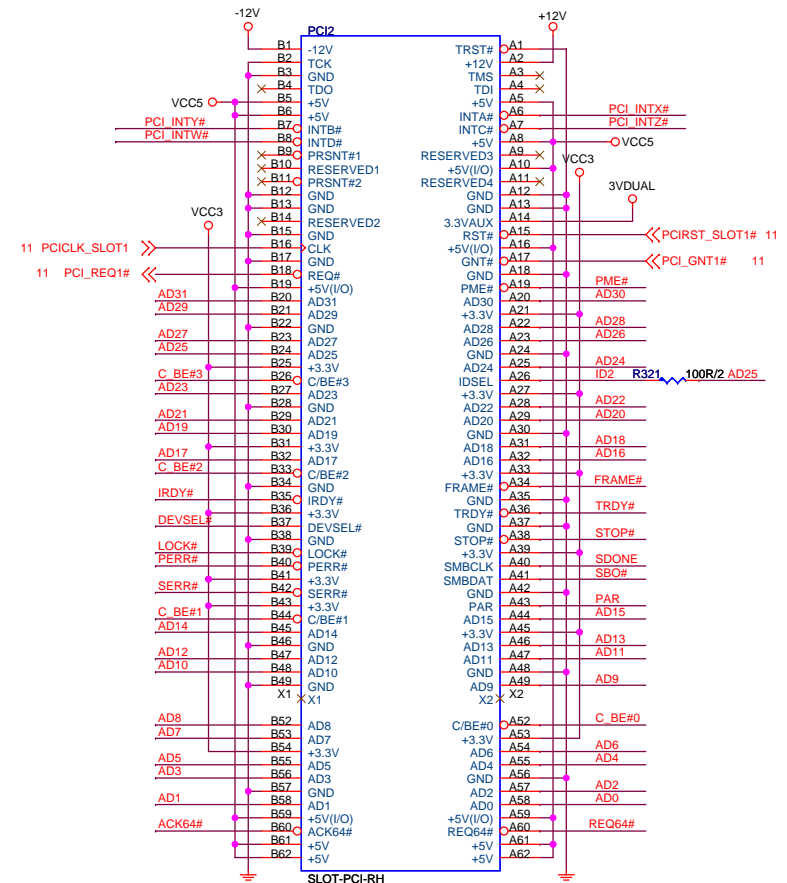


PCI SLOT 1 (PCI VER: 2.2 COMPLY)



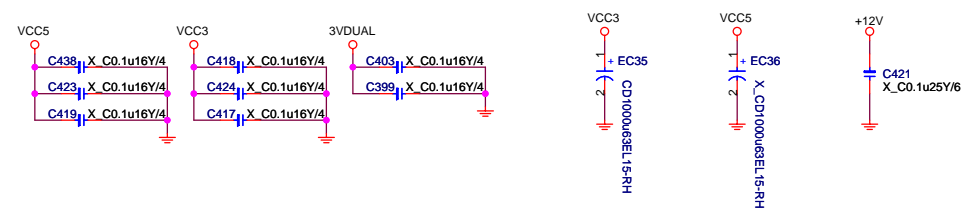
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INT W# X# Y# Z#
PCICLK_SLOT1

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

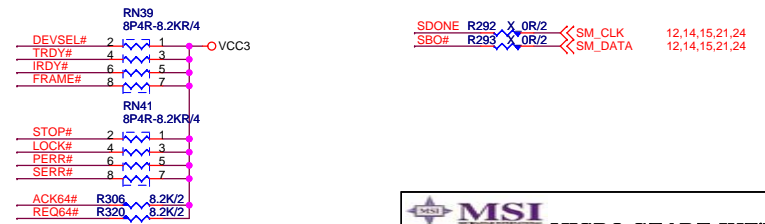


IDSEL = AD25
PCI_REQ1# PCI_GNT1#
INT X# Y# Z# W#
PCICLK_SLOT2

PCI SLOT DECOUPLING CAPACITORS



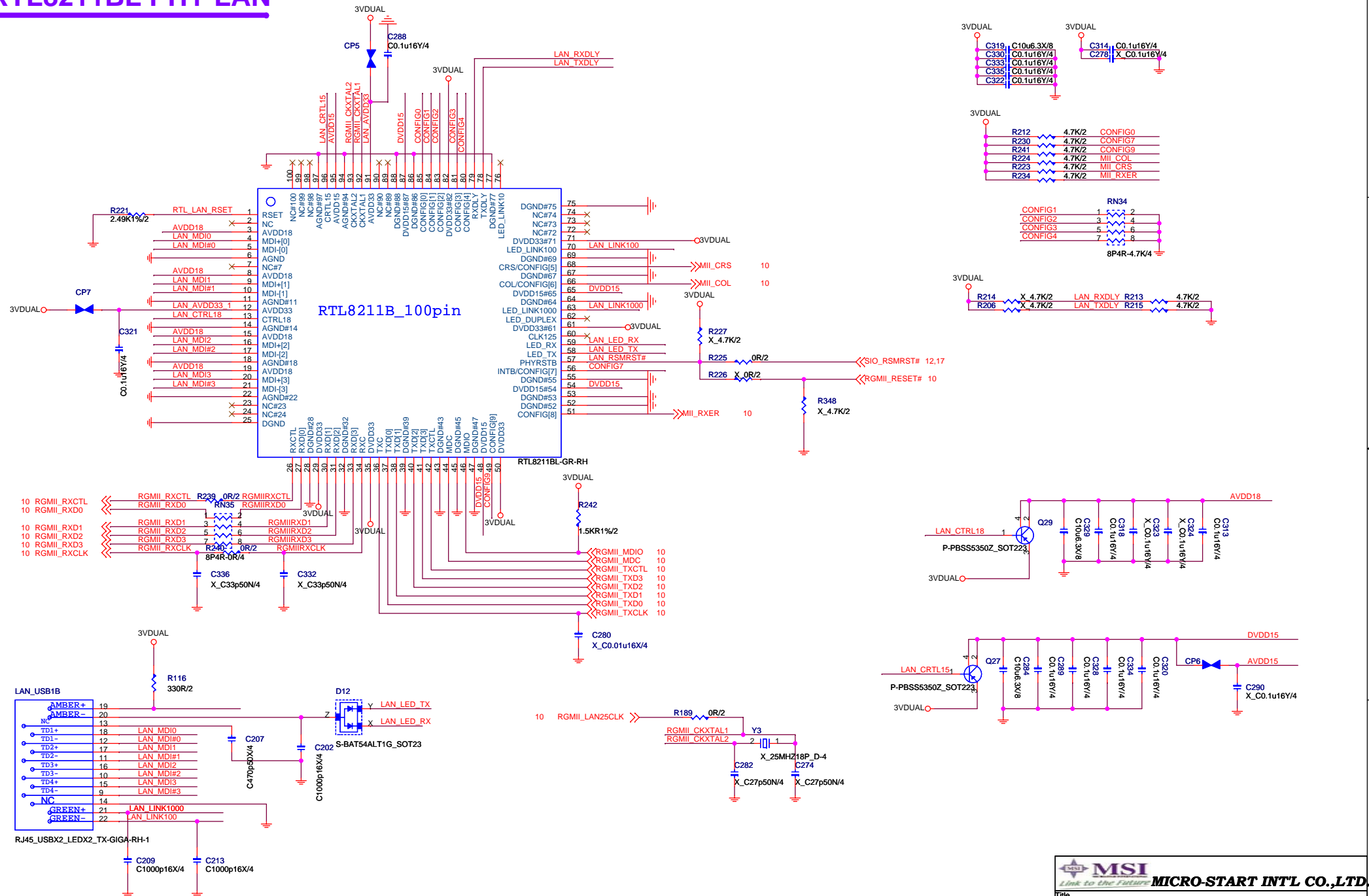
PCI PULL-UP / DOWN RESISTORS



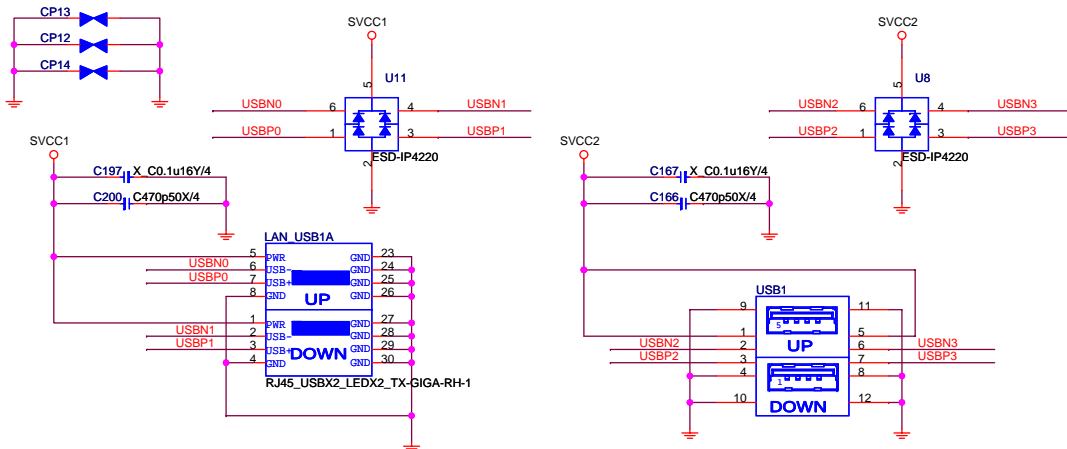
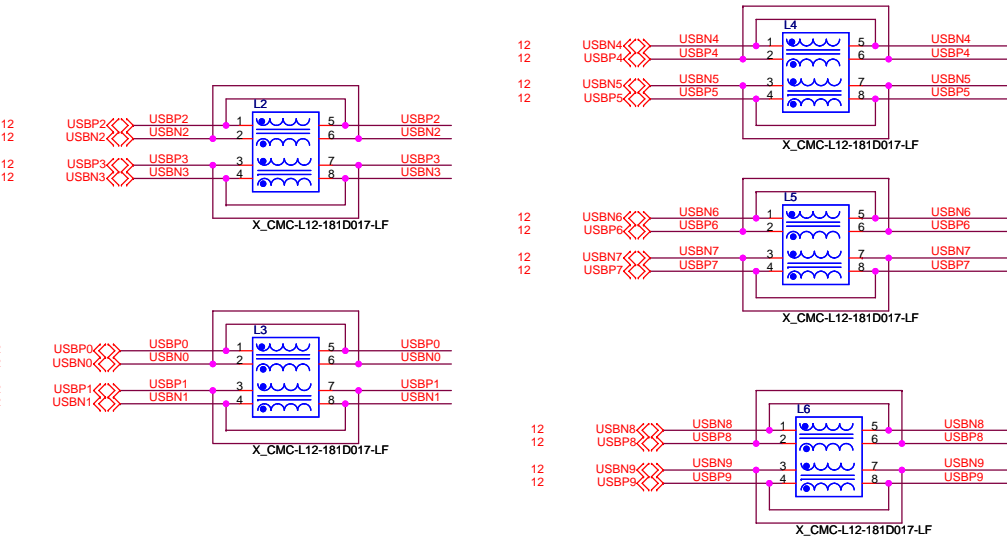
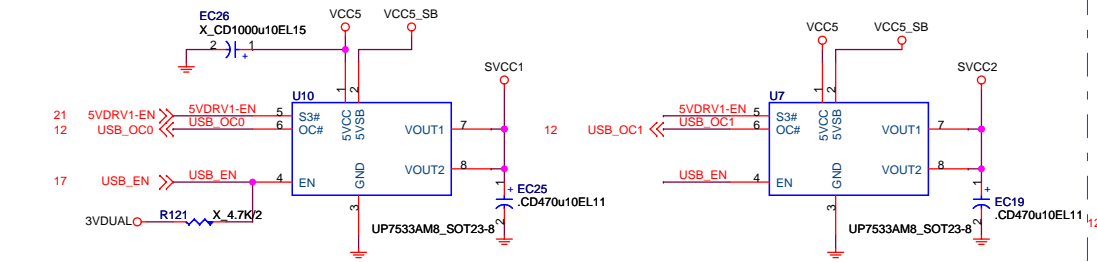
MICRO-START INT'L CO.,LTD.

Title PCI Slot 1 & 2		
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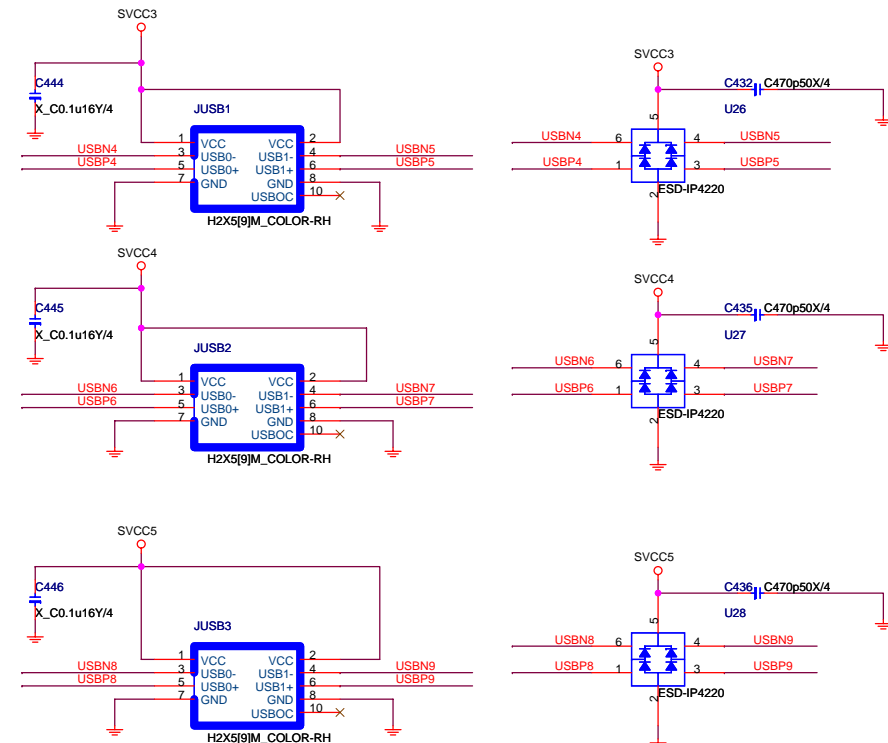
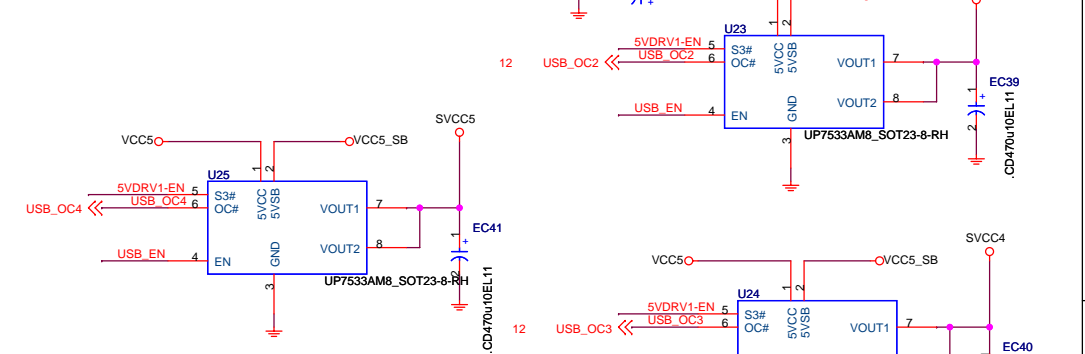
RTL8211BL PHY LAN



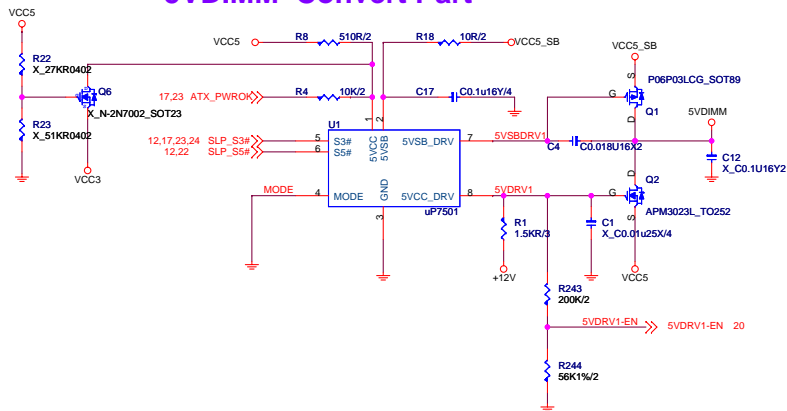
REAR USB Power



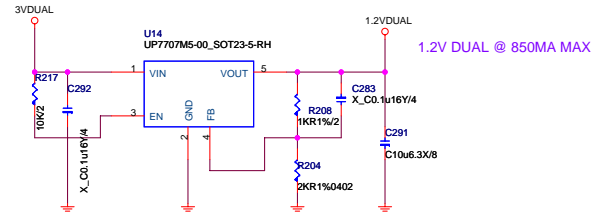
Front USB Power



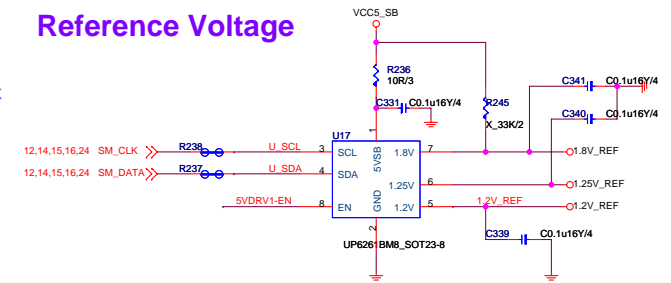
5VDIMM Convert Part



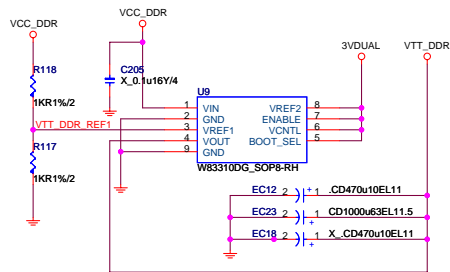
1.2VDUAL Convert Part



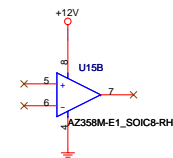
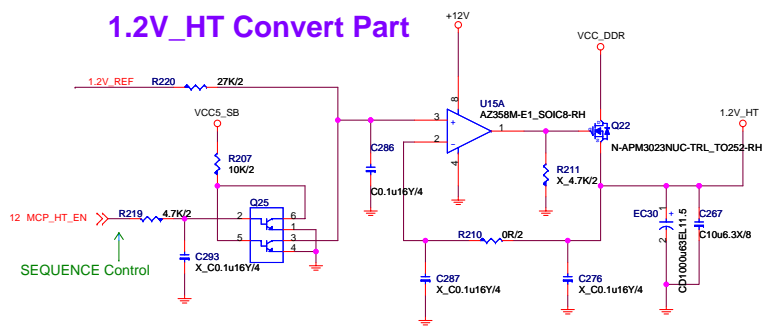
Reference Voltage



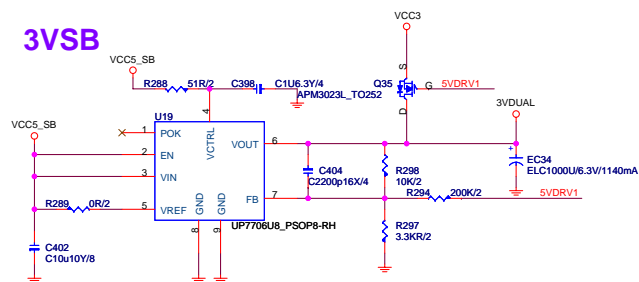
VTT Convert Part



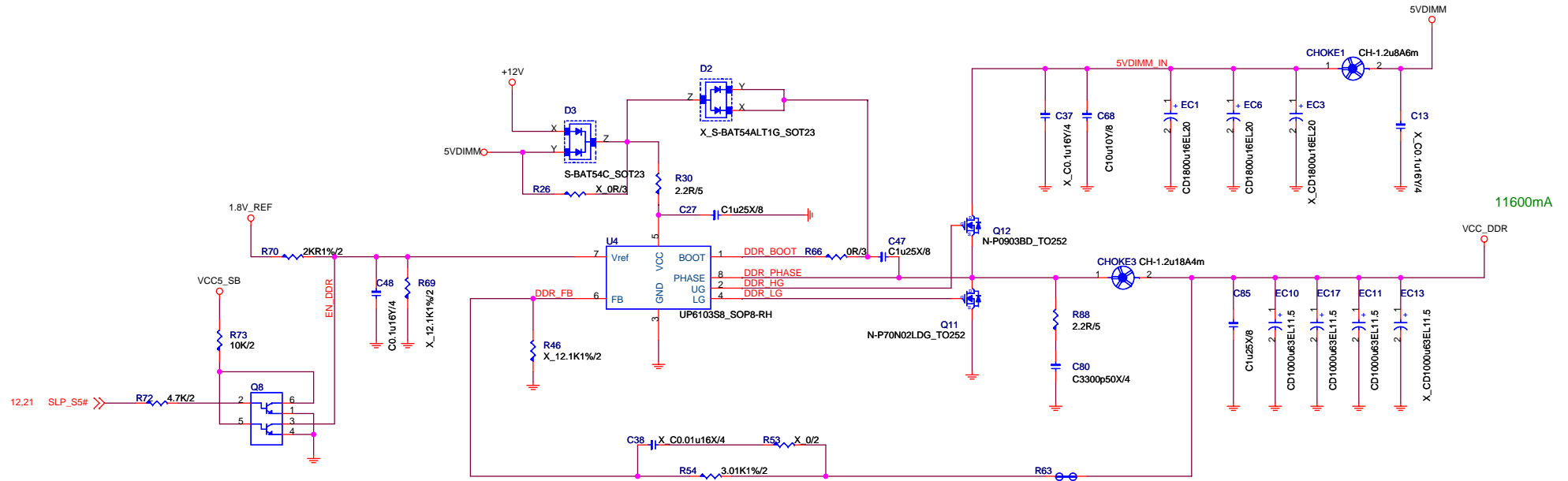
1.2V_HT Convert Part



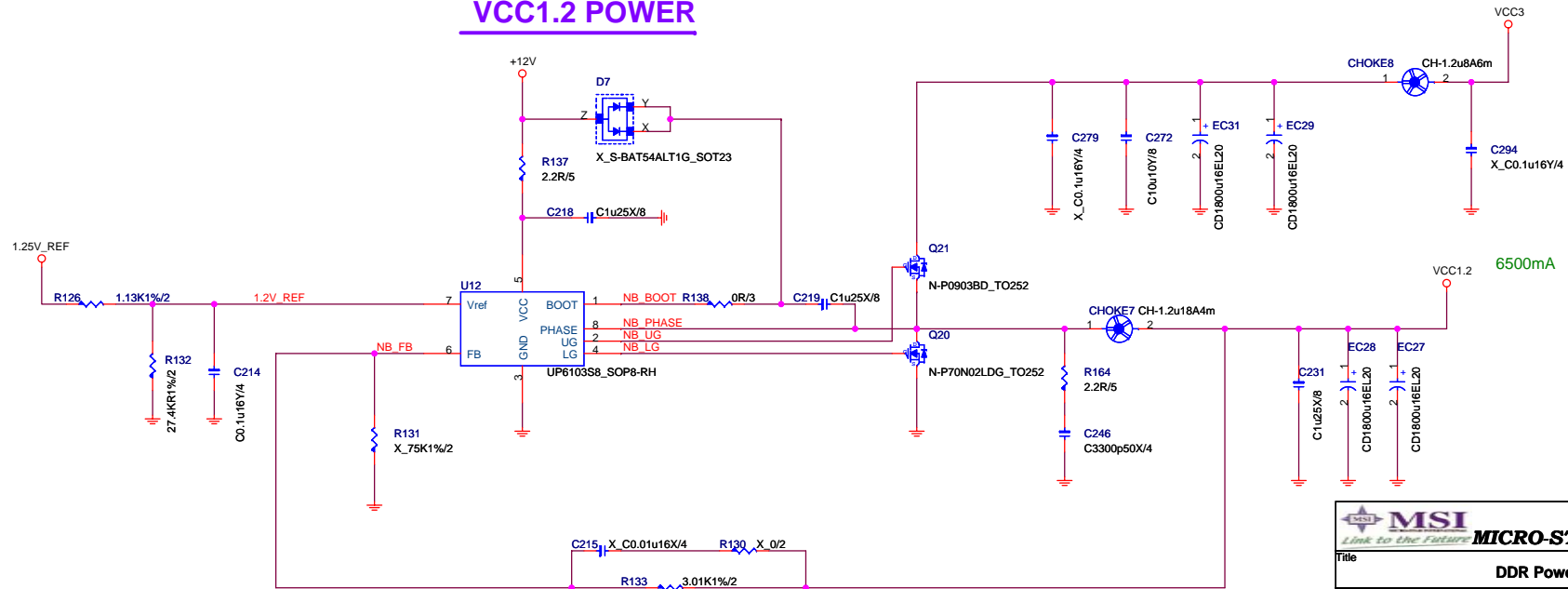
3VSB

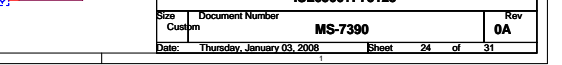
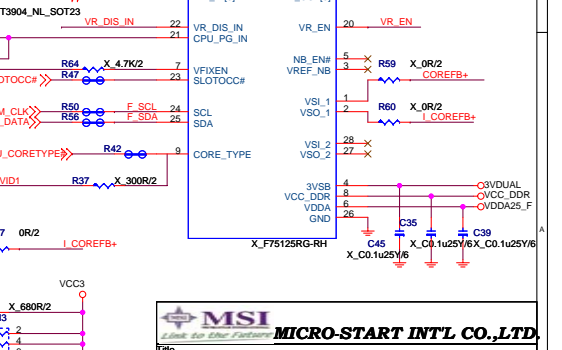
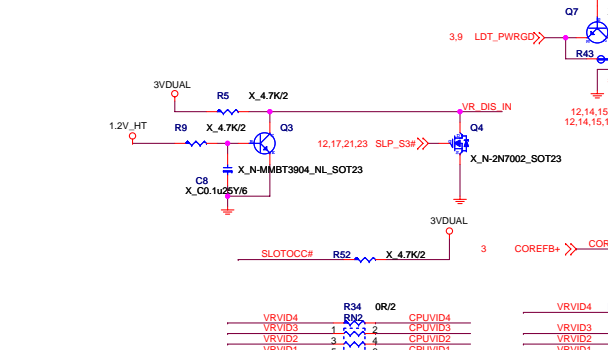
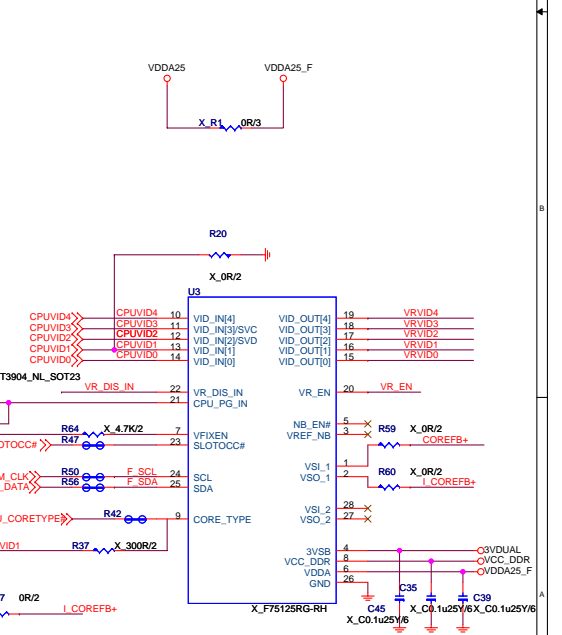
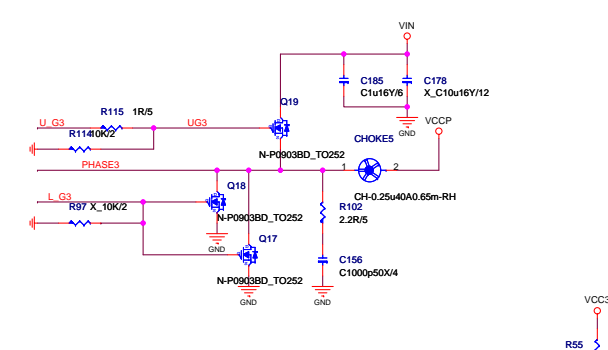
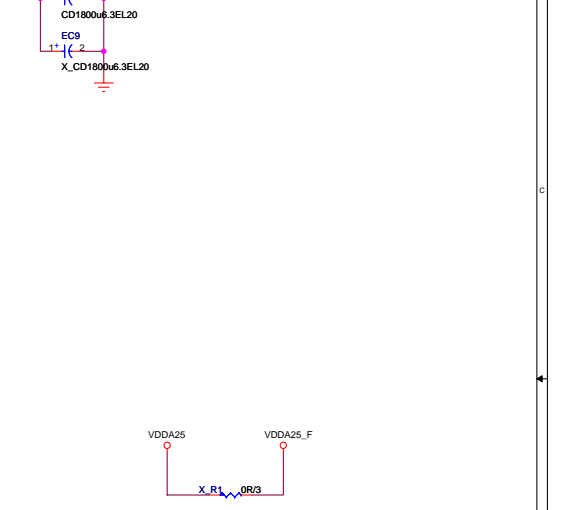
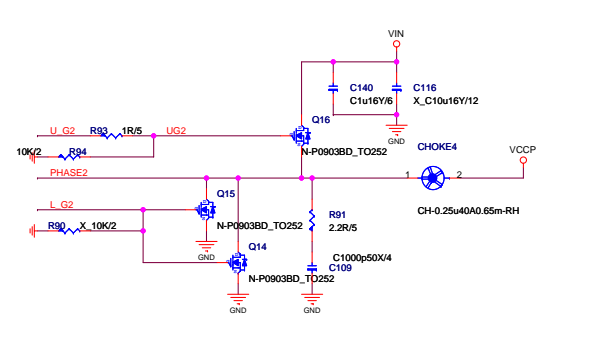
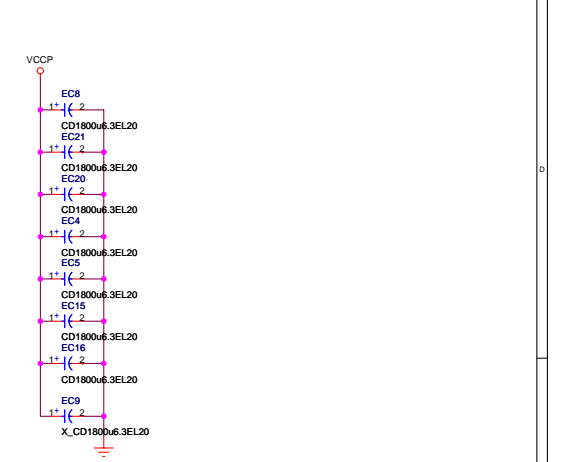
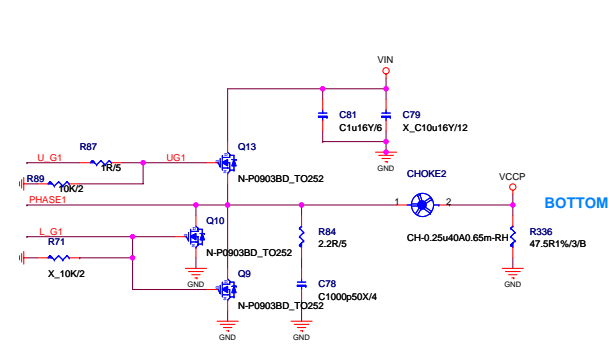
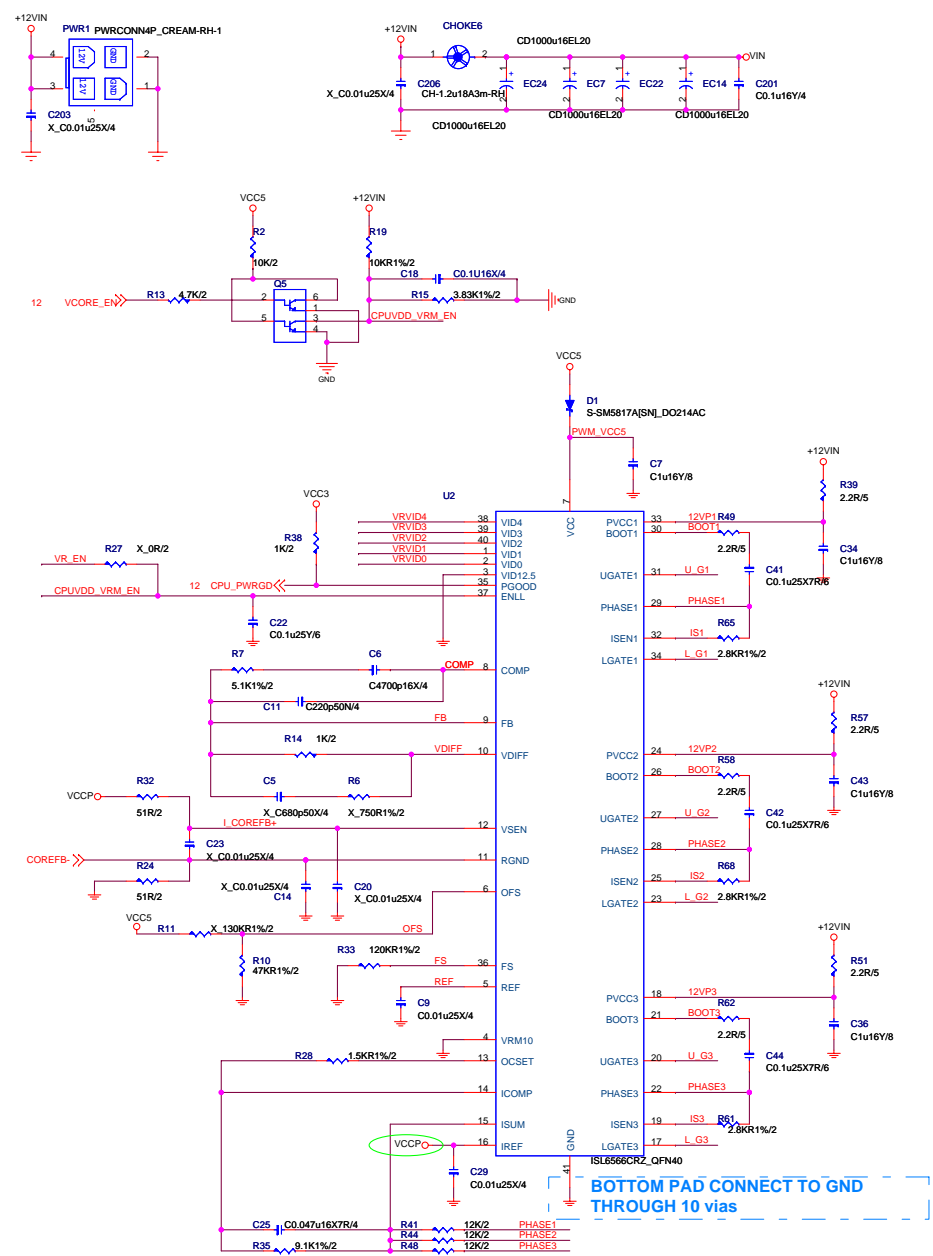


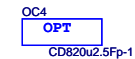
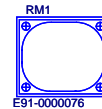
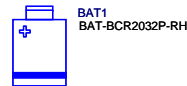
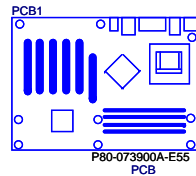
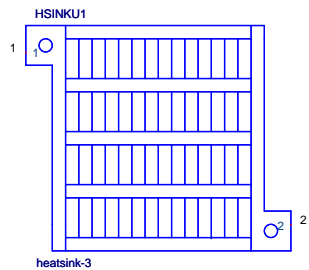
DDR II 1.8V POWER



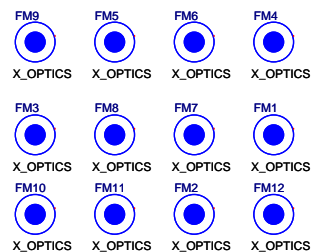
VCC1.2 POWER



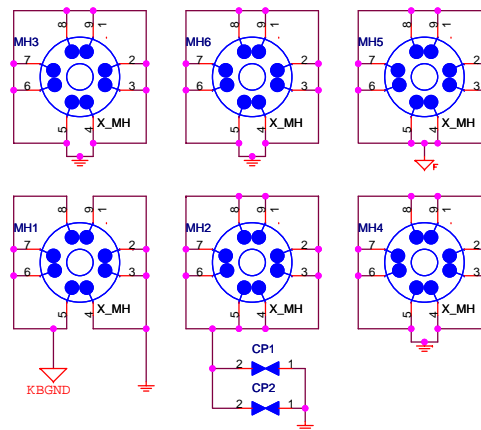




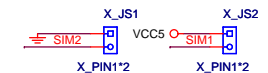
Optics Orientation Holes



Mounting Holes




Simulation

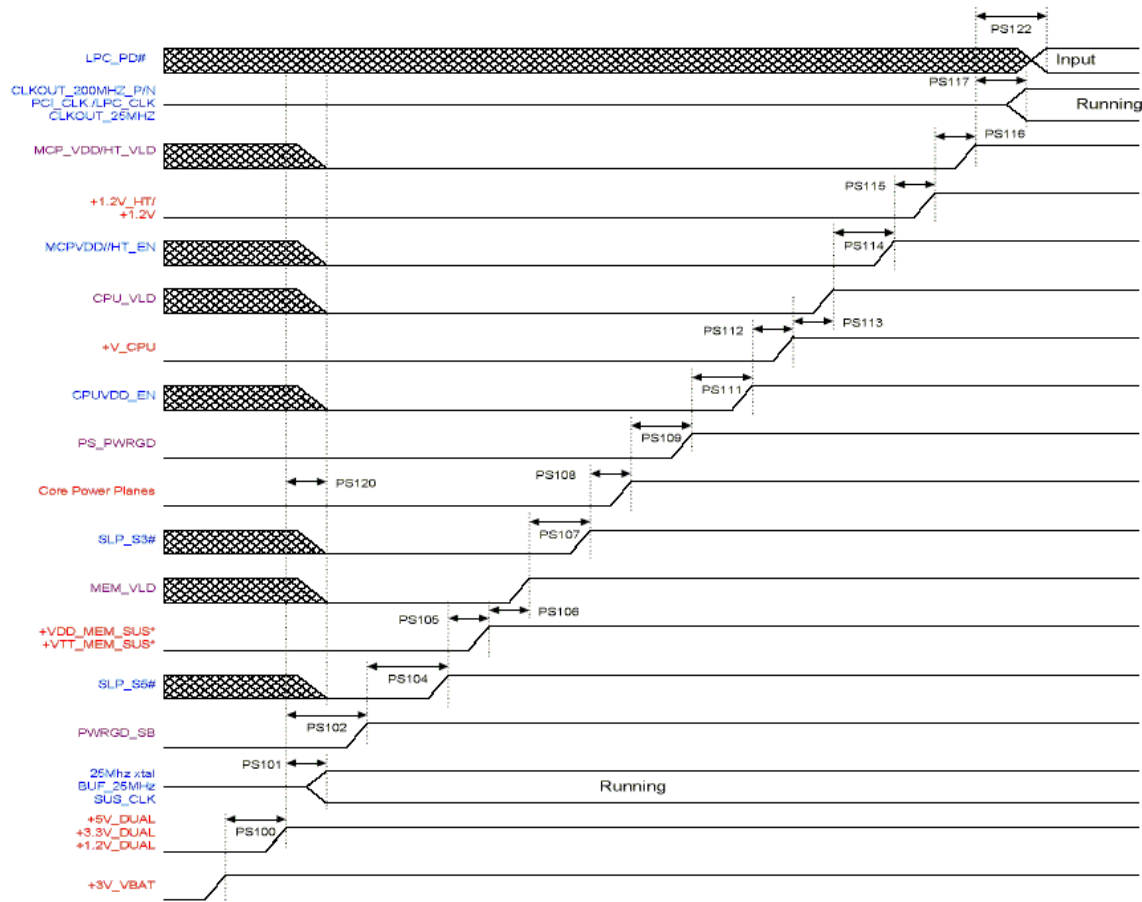


Model option table

Model type	Function	BOM Config	ERP BOM No.
MS-7390	MCP65P+RTL8211BL+ALC888+2PCI+2PCIEX8+2PCIEX1+2PS2+10USB+1COM+1Print Port+1Audio+RJ45+ OSC Cap	Cfg-7390	601-7390-A10 601-7390-01S



 MSI <i>Link to the Future</i>		MICRO-START INT'L CO.,LTD.	
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Power Planes are in Red MCP output signals are in Blue Motherboard generated inputs to MCP are in Purple

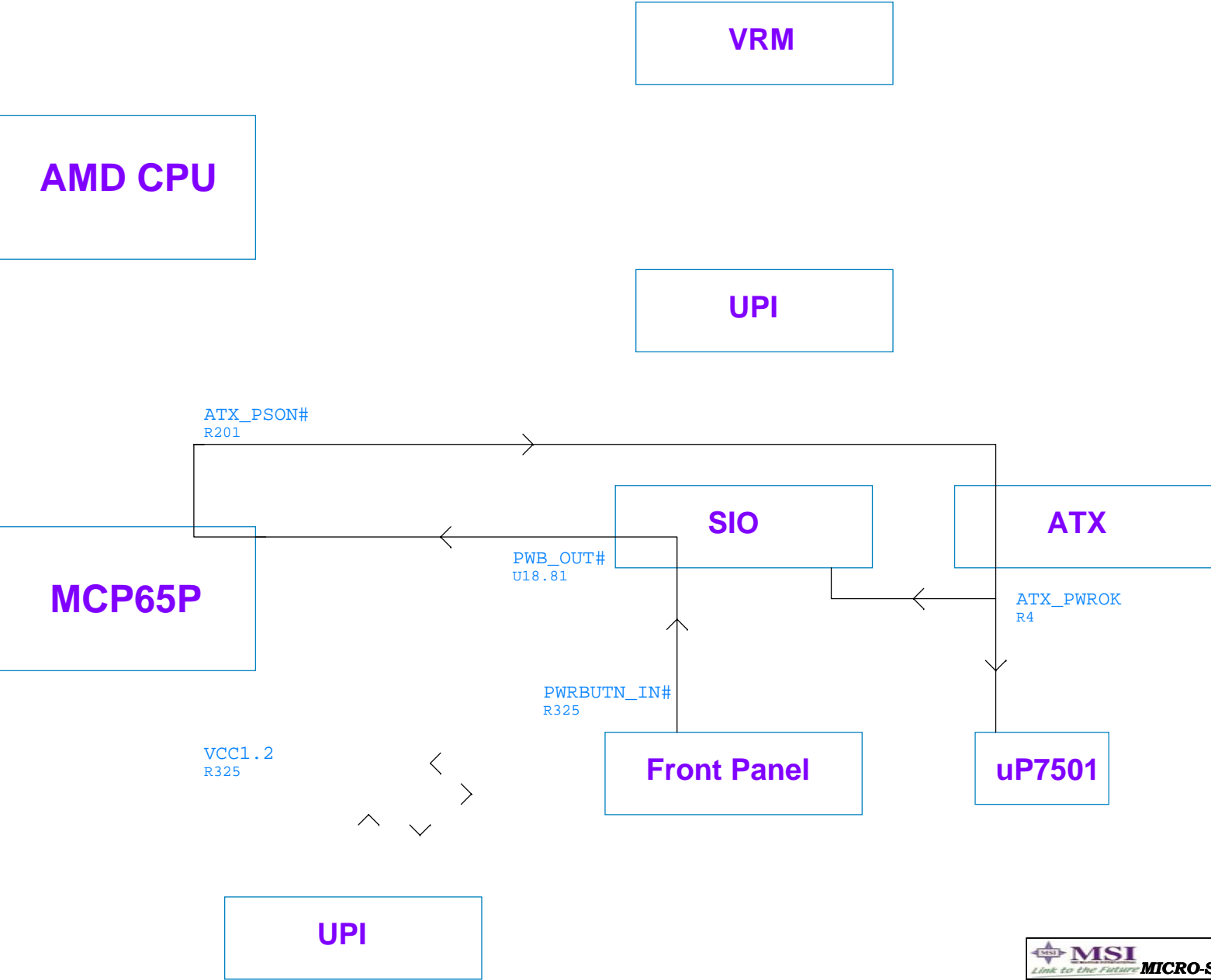
*Core Planes include:
All power planes without _DUAL or _SUS in the name except:
CPU Core Power Plane
1.2V_HT
and Optionally the MCP Core voltage plane.

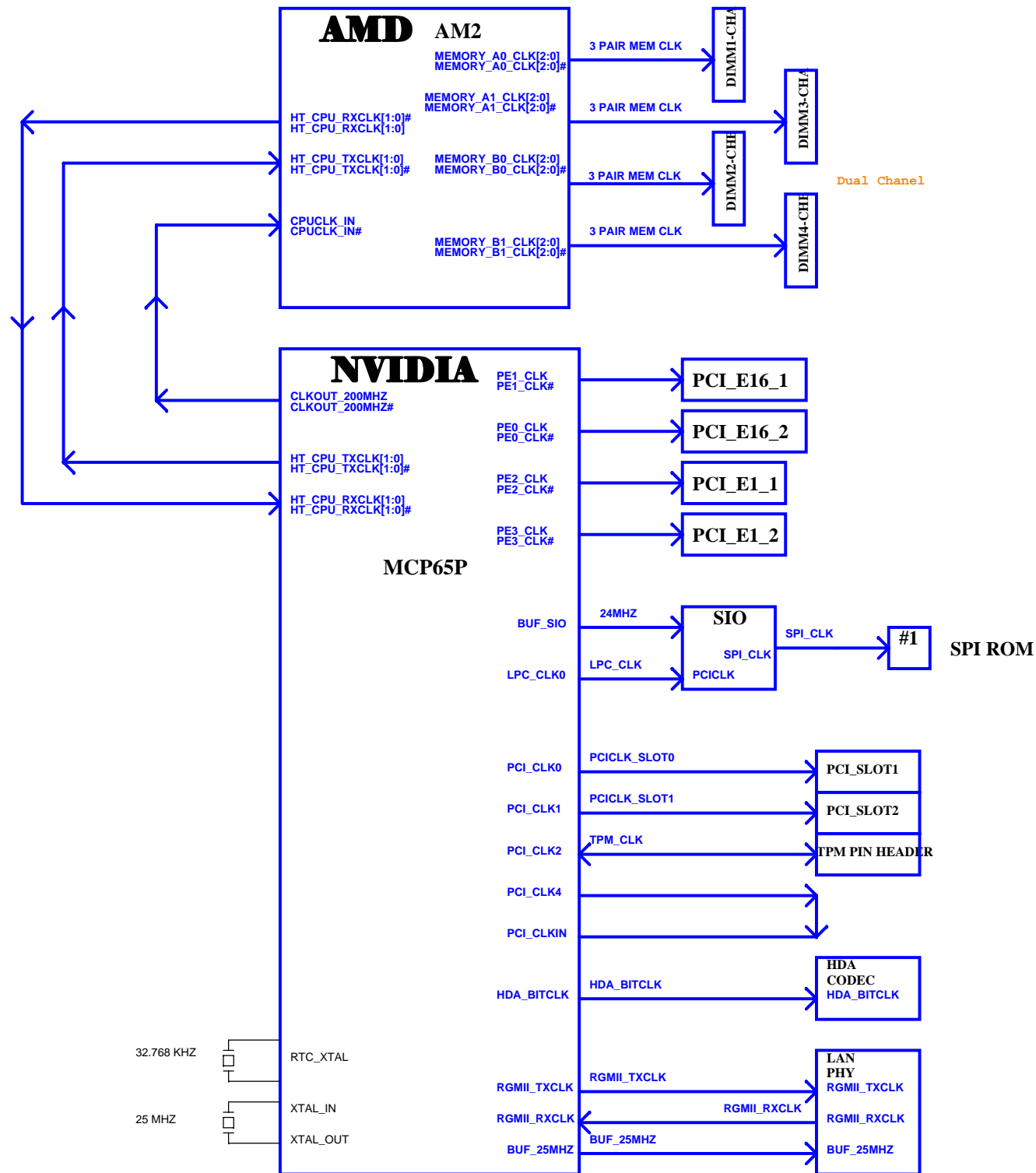
*Memory Power Planes vary with the memory standard.
DDR I = 2.5, 1.25V
DDR II = 1.8, 0.9V

Sym	Parameter	Min	Max	Units	Notes
PS100	+3V_VBAT active to +V_DUAL active	0		ms	1, 5
PS101	+V_DUAL active to XTAL OSC active	0	10	ms	1, 2
PS102	+V_DUAL active to PWRGD_SB assert	10		ms	5
PS104	PWRGD_SB assert to SLP_S5# de-assert	11	12	ms	3
PS105	SLP_S5# de-assert to SUS Powers valid	0		ms	4, 6
PS106	SUS Powers valid to MEM_VLD assert	0		ms	
PS107	MEM_VLD assert to SLP_S3# de-assert	10	15	ms	3
PS108	SLP_S3# de-assert to CORE Power Planes valid	0		ms	1, 4, 9
PS109	CORE Power Planes valid to PS_PWRGD assert	0		ms	
PS111	PS_PWRGD assert to CPUVDD_EN assert	50	73	ms	7
PS112	CPUVDD_EN assert to +V_CPU valid	0		ms	4
PS113	+V_CPU valid to CPU_VLD assert	0		ms	
PS114	CPU_VLD assert to MCPVDD/HT_EN assert	10	15	ms	3, 9
PS115	MCPVDD/HT_EN assert to +1.2V_HT valid	0		ms	4, 9
PS116	+1.2V_HT valid to MCPVDD/HT_VLD assert	0		ms	
PS117	MCPVDD/HT_VLD assert to CPU and LPC clocks active		33	ms	8
PS120	+V_DUAL valid to power plane controls valid		10	ms	
PS122	MCPVDD/HT_VLD to power state controls de-assert			ms	10


Notes:

- +3V_VBAT can never be invalid when any of the DUAL planes are valid. Also, the VCC CORE planes must never be valid when +3V_VBAT or any of the DUAL planes are invalid. The MCP65 is designed based upon the assumption that the power planes will sequence in this order. If the power plane sequence is not followed, the MCP65 may fail. The motherboard is responsible for ensuring this ordering.
- As soon as DUAL power is received, the main 25 MHz oscillator circuit becomes active, BUF_25MHZ will begin driving a buffered version of the 25 MHz XTAL input, and SUSCLK will begin driving a 32 kHz clock.
- MCP65 internal timed delay to ease motherboard power sequencing requirements.
- Motherboard power supply design and capacitive loading determine the delay from the SLP#/EN signals to the 90% valid time of the associated power plane. There is no required time for the motherboard design to meet. The power plane must not be valid before being enabled. S3 resume time will be affected by these delays, so the motherboard designer should strive to minimize this delay as possible.
- If +3.3V_VBAT and +V_DUAL are ramping at the same time (connected together), then PWRGD_SB must be sufficiently delayed (PS102 timing) to allow time for the 32 kHz clock to settle. The motherboard is responsible for ensuring that the 32 kHz clock crystal is settled before PWRGD_SB is asserted. Otherwise, the MCP65 may fail to power up.
- K8 requirements indicate that +VDD_MEM_SUS and +VTT_MEM_SUS must ramp together and never be more than 1.3 Volts apart.
- PS_PWRGD is debounced for 40ms before registering high internal to the MCP65. This allows for silver box based PWRGD signals to drive the PS_PWRGD input directly.
- There is no minimum time, some clocks may start before HT_VLD goes high (negative minimum time). The maximum is based on the internal delay that is added by MCP between power and the enabling of internal PLL logic. All clocks derived from a PLL will not be active until after PS_PWRGD/CPU_VLD/MCPVDD/HT_VLD/PWRGD_SB signals are asserted. Note that BUF_25MHZ is not derived from a PLL and will be active before MCPVDD/HT_VLD goes high.
- HT Link's VDD (+1.2V_HT) and MCP65's core +1.2V power rails can come from the same regulator. In this case, MCP65's core power will not be enabled until MCPVDD/HT_EN is asserted.
- By default LPC_PD# will be an input on power up.





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0A2

1. List and change the 5020 2007.11.30


0A3

- 1.Reserved C51.C84.C180.C198.C139.C120.C171.C46.C32.C230.C238.C236.C222.C223.C208.C3.
- 2.Stuff C169.C186.C196.C199.C506.C504.C502.C508C514.C517.C525.C502.RT1.R2683.C350.C313
- 3.Change PCI_E16_1 & PCI_E16_2 to N11-1640421-K06

1.0

1. Stuff C339 to 0.1uf cap. 2007.112.17
2. Stuff R222\R218\R209\Q26\Q28;Change R232\R216 's footprint to R0402 2007.12.28
3. Change C332\C336 to reserved 2007.12.28
4. Add R349\R350 for AMD CPU 2007.12.28
5. Change C207 to 470pf for EMI; Remove C132 2007.12.29
6. Change R190 to 0ohm for RGMII_CKXTAL1 fall time ovre spec . 2007.12.29
7. Change Audio Jack's Part No to N54-26F0201-S42 2008.01.02
8. Add Power Solutin: Stuff C5,R6,R11; Stuff R10 to R11-0473T12-W08; C25 change to X7R; C41, C42, C44 change to X7R. 2008.01.02

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